ISSN 2321 – 2004
ISSN 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 1, Issue 6, September 2013

MEMORY DEBUG USING BIST

Ms.Syed Sumera Ali

Assistant professor, Dept. of Electronics & Telecommunication, MGM's College of Engineering. ,Nanded-India

Abstract : Built –in self test (BIST) are best tested in Embedded Memories such as RAMs and ROMs. The use of BIST is for manufacturing or production testing with additional features for diagnostics and debug [1].This paper present a study on memory debug methodology using BIST in system-on-chip (SOC) product development and yield ramp-up and describes diagnosis techniques during rapid development of semiconductor memories for catching the design and manufacturing failures and improving over all yield and quality[2]. It also covers MARCH based memory diagnosis algorithm which locate fault cells also identified their types, using the proposed algorithm stuck-at-faults, state coupling faults, transition faults can be distinguished. With all of these, defect diagnosis and Field application (FA) engineer can be performed automatically using the fault patterns, reducing the time in yield improvement [3]. The main purpose of this algorithm is accelerating fault diagnosis for semiconductor memories. Design is described using verilog HDL simulation is carried out using Modelsim simulator synthesis is done using Xilinx ISE Implementation is done on Spartan 3e FPGA .

Keywords : Memory debug algorithm , March 17n algorithm , BIST

I. INTRODUCTION

Memory diagnosis becoming a critical issue, so far as manufacturing yield and time to-volume of SOC product are concerned [5]. The BIST methodologies presented increase testability of embedded memories that go into present day SOC. Memory BIST provides a good way to protect the intellectual property contained within the core. Memory failures can be single or multiple bits. It is desirable to diagnose and track all types of failures [6].

Failure Analysis can be used to identify the defects causing the yield loss. FA engineer first detects and locates the faulty cell or region and then performs a series of physical de-processing, e-beam probing or electron microscope inspection. However without proper methodologies and tools it is more and more difficult to perform the defect-level testing and diagnostics as it get into the deep-submicron age. Bitmaps and wafer maps are the tools that have been commonly used in FA .For memories, fault model are defined at the functional level. Based on the faulty circuit behavior, a test algorithm can be developed to detect the faults that are modeled .The quality of test algorithm is determined by its length and fault coverage. Memory fault diagnosis procedure also has been developed based on functional model. With the advent of new technology, i.e. Using CMOS VLSI design methodology could design and fabricate ICs without spending much time .Also designer could able to develop CAD/CAE (Computer Aided Design/Computer Aided Engineer) tools for design electronics circuit with assistance of software programs .The knowledge of VLSI design , design methodologies of software and hardware tools for implementation of this paper are required .

II . MEMORY TESTING ALGORITHMS

The table I gives the comparison of six testing algorithms to test four memory fault models Stuck At Faults(SA), Transition Faults(TF), Coupling Faults(CF), Data Retention Faults(DRF). The best is March C- which covers all faults with small number of patterns. MATS used smallest number of patterns but only detect Stuck At Fault, (SAF).

Algorithms	No. of Patterns, n (complexity)	Detectable Faults		
		SAF	DRF	CF
MARCH A	15n	All	All	All
MARCH B	17n	All	All	All
MARCH C	11n	All	All	All
MARCH C-	10n	All	All	All
MATS	4n	All		
MATS +	5n	All		

TABLE I.THE SIX TEST PATTERN ALGORITHMS

ISSN 2321 – 2004
ISSN 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 1, Issue 6, September 2013

III.BIST MARCH 17N ALGORITHM

The March Algorithm consists of several March elements , Separated by semicolon. Up-arrow stands for ascending order of address sequence , Down-arrow stands for descending order.Inside parenthesis read write operations[4].

March signature is use to represent the result from all operations in the test algorithm which are either correct (represented by 0) or incorrect (represented by 1) .

A. NOTATION OF MARCH 17N ALGORITHM

⇑ : address 0 to address n-1

⇓ : address n-1 to address 0

w0 : write 0

w1 : write 1

r0 : read a cell whose value should be 0

r1 : read a cell whose value should be 1

The March 17N memory BIST Architecture consists of 3 different blocks i.e.BIST register block, BIST state machine block and memory block.BIST register further consists of three registers BIST start register ,BIST flag register, BIST communicate status register. Four memories are used for better understanding however a provision for further increment of memories is provided. Each of blocks are designed separately using a verilog HDL code and then verified individually. After designig of all blocks, these blocks are integrated to perform the memory diagnosis operation.

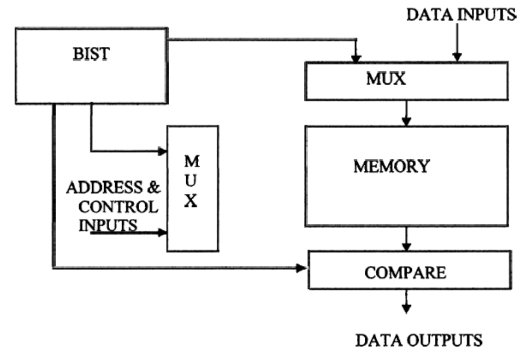

Fig1. Memory BIST Architecture

Registers are usually implemented in register file or individual Flip Flop, High-speed core memory, thin film memory and other ways various machines. The BIST consist of the following registers. BIST_START_REGISTER is of 32bit used as input under the read/write mode.

BIST_FLAG_REGISTERis of 32bit used as output under read only mode .

IV. BIST STATE MACHINE

Finite state machine or finite state automation (FSM) is a model of behavior composed of a finite number of states , transitions between those states ,and actions. There are two types of state machine (a) Moore machine; this model is a simplification of behavior example is Elevator door. (b) Mealy machine, use of this model leads often to a reduction of the number of states.

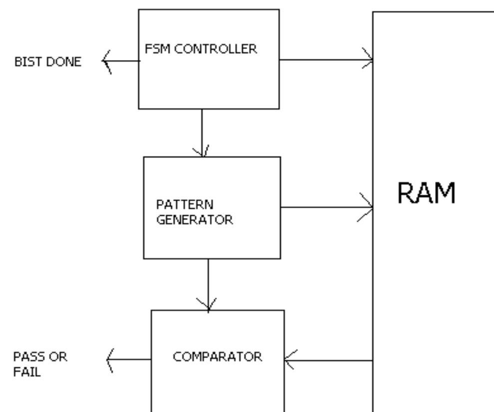

Figure 2. Bist controller

The BIST_START_REGISTER will trigger the state machine and it starts performing march 17n memory BIST algorithm. It starts performing write zero read zero , write

ISSN 2321 – 2004
ISSN 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 1, Issue 6, September 2013

one and read one operation as described by the protocol.There are 8 different kinds of read and write operation required to be performed as part of the memory BIST protocol.State machine consist of following states:

1. ST_IDLE
2. ST_1_W0_A
3. ST_2_R0W1R1_A
4. ST_3_R1W0R0_A
5. ST_4_R0W1_A
6. ST_5_R1W0R0_D
7. ST_6_R0_A
8. ST_7_ROW1R1_D
9. ST_8_R1_A
10. ST_STATUS

IV.SIMULATION RESULTS

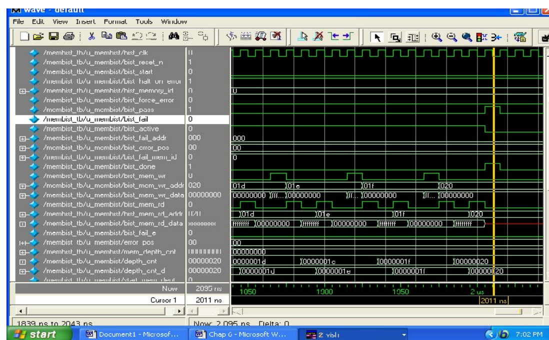

Figure 3. Simulation Waveform

The above figure shows Simulation waveform of MBIST State Machine for MBIST test case PASS. When all the states of writing 0's or 1's and reading 0's or 1's from all the memory locations completes successfully then MBIST state machine generates a signal of MBIST PASS and MBIST DONE. Similarly Simulation waveform of MBIST State Machine for MBIST FAIL. While reading 0's or 1's from any memory location, if the state machine encounters an error then it generate a signal of MBIST FAIL. Likewise MBIST PASS and MBIST FAIL simulation can be done .Consequently Simulation of memory block for read and write operation can find. In this when write signal is high, memory write operation takes place for the specified memory addresses and data. When read signal is made high, data from the specified memory addresses is read.

V. CONCLUSION

The technique presented in this paper is not only increases the speed of detecting the faults but also reduces the cost with optimized design. It covers all kinds of fault and guarantees of fault free memories in SOC. March 17N algorithm is much faster and covers the faults of semiconductor memories accurately [8]. It is also used to ramp-up the yield of coproduction. Here we have simulated the BIST architecture for only for four memories it can be upgraded to any number of memories depending upon the requirement and target board availability. Also this paper is very first step for new technology called Built-in self repair (BISR)[9] .This paper can upgrade interms of power using one hot coding or gray code in BIST state machine.

ACKNOWLEDGMENT

I express my sincere thanks to Dr. SYED ABDUL SATTAR (H.O.D of ECE Dept.), Dr . SHAH AQUEEL AHMED (H.O.D of EIE Dept .) , PROF. Khaja Mujeebuddin Quadri they not only encouraged me to take up this topic but also given their valuable guidance in assessing facts and arriving at conclusions.

REFERENCES

[1] M. E. Levitt, "Designing UltraSparc for Testability," IEEE Design and Test of Computers, Vol. 14, No.1, pp. 10-17, January - March 1997.
[2] K. Kinoshita, K. K. Saluja, "Built-In Testing of Memory using an On-Chip Compact Testing Scheme," IEEE Transactions on Computers, Vol. C-35, No. 10, pp. 862-870, Oct. 1986.
[3] K. T. Le, K. K. Saluja, "A Novel Approach for Testing Memories using a Built-In Self Testing Scheme," Proc. IEEE International Test Conference, pp. 830-839, 1986.
[4] P. H. Bardell, W. H. McAnney, and J. Savir, Built-In Test for VLSI: Pseudorandom Techniques, John Wiley and Sons, 1987.
[5] R. David, A. Fuentes and B. Courtois, "Random Pattern Testing Versus Deterministic Testing of RAMs," IEEE Transactions on Computers, Vol C-38, No. 5, pp. 637-650, May 1989.
[6] R. Dekker, F. Beenker and L. Thijssen, "Realistic Built-In Self Test for Static RAMs," IEEE Design & Test of Computers, Vol. 6, No. 1, pp. 26-34, Feb. 1989.
[7] B. Nadeau-Dostie, A. Silburt and V. K. Agarwal, "Serial Interface for Embedded-Memory Testing," IEEE Design & Test of Computers, Vol. 7, No. 2, pp. 52-63, April 1990.
[8] M. Nicolaidis, "Transparent BIST for RAMs," Proc. IEEE International Test Conference, pp. 598-607, Oct. 1992.
[9] Essentials of Electronic Testing for Digital, memory & Mixed-Signal VLSI Circuits, MichaelL Bushnell and Vishwani D. Agrawal, Boston: Kluwer Academic Publishers, 2000.

BIOGRAPHY

Ms.Syed Sumera Ali, MTech(DSCE) , BE(ECE) , D.E.E, Assistant Professor, **Research Interest :** Biomedical Electronics. **Awards :** International paper presentation award (STAR OF THE MGM)